Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A latch circuit, comprising:

a bistable pair of transistors with both transistors connected directly between a reset switch and a first node, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and

a vertical latch having a first transistor ~~and~~ connected directly to a second ~~transistor and~~ transistor, said second transistor connected directly ~~between~~ to said first ~~node and~~ node, said first transistor connected directly to a second node, said first transistor connected to said first port so that, when said first transistor is turned on, a current flows through said first transistor and said first port, wherein said first transistor is a first type, said second transistor is a second type, and said first type is different from said second type.

2. (Previously Presented) The latch circuit of claim 1, wherein said first transistor is a MOSFET.

3. (Original) The latch circuit of claim 1, wherein said reset switch is a microelectromechanical reset switch.

4. (Previously Presented) The latch circuit of claim 1, wherein said vertical latch is for decreasing the time necessary for said first port to reach a steady state voltage in response to said first current signal received.

5. (Original) The latch circuit of claim 1, further comprising a vertical latch reset switch connected to said vertical latch.

6. (Previously Presented) The latch circuit of claim 1, further comprising a second vertical latch connected between said first node and said second node, and connected to said second port.

7-21. (Canceled)